Development and Investigation of Two Optimized Soft Switching Pulsed Power Resonant Converters for RF Applications

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Abstract

This paper focuses on the closed-loop voltage control of two classical soft switching pulsed power resonant converters for radio frequency applications. Based on the optimization algorithms proposed in the previous work, the two converters are designed to produce a series of "long pulse" voltage waveforms, each one rated at 9MW, 120kV, 1ms, 1% voltage ripple. A novel PI + Repetitive Control strategy is employed for voltage pulse regulation, resulting in a fast rise time, reduced overshoot and constant amplitude. The soft-switching of semiconductor devices is ensured throughout the pulse by a combined frequency and phase shift modulation, in order to maximize the system conversion efficiency.

I. INTRODUCTION

Long pulse modulators used for high energy particle acceleration experiments are required to generate a series of high quality voltage pulses to power a radio frequency (RF) tube, each pulse lasting several milliseconds in length. The magnitude of high power, high voltage pulses needs to be stable and predictable so that any variation in it has a limited and acceptable influence on the acceleration. A stringent pulse dynamics (that with a fast rise time but no overshoot) is also demanded to ensure high conversion efficiency. The current generation of those modulators [1] is based on 50/60Hz, line frequency technology, which requires bulky passive components and bouncer circuits to meet the strict pulse quality requirements and a crowbar circuit for the purpose of load protection from large energy storage.

In the past decade, to meet the increased demand of developing compact modulators with high efficiency and high power density, the resonant technology has been considered as a promising solution. Based on a series resonant parallel loaded (SRPL) approach, two classical converter modulators have been proposed for pulsed power applications, which are the Y-point connected part resonant converter modulator [2] and the three-phase fully resonant converter modulator [3]. The optimization algorithms presented in [4] can be used to simplify and speed up the design process of the two converters. Several topology variants, such as single phase [5], three-single phase [6] and single phase with a multi-core transformer [7], have been developed for different research directions to enable practical implementations.

Due to the resonant stage introduced and the use of varying frequency operation, the voltage control of those pulsed power resonant converters is inherently difficult. Generally, a feed-forward control is utilized to regulate the voltage pulses [3, 8]. However, it has two main limitations. One is that it requires considerable tuning work to obtain a qualified voltage pulse (i.e. short rise time and constant amplitude). Another is that in case of parameters variations, it is unable to react to the change and modify the output. Hence, the tuning procedure needs to be repeated. With the aim of overcoming those limitations, a multi-variable state feedback controller was developed in [9]. Although the controller can regulate the pulse amplitude effectively, the rise time was longer than expected, due to the presence of the full state observer.

This paper focuses on the closed-loop control of the pulsed power resonant converters. Based on the optimization algorithms proposed in the previous work [4], the two converters are designed to produce a series of "long pulse" voltage waveforms, each one rated at 9MW, 120kV, 1ms, 1% voltage ripple. In order to obtain good control performance both in transient and steady state conditions, a novel PI + Repetitive Control (RC) strategy is employed for voltage pulse regulation, resulting in a fast rise time, reduced overshoot and constant amplitude. The soft-switching of semiconductor devices is ensured throughout the pulse by a combined frequency and phase shift modulation to maximize the system conversion efficiency.

II. CONVERTER TOPOLOGIES

Fig. 1 shows a generalized block diagram of the pulsed power resonant converter modulators. Supplied by the grid, a rectifying stage is used to charge a DC-link capacitor bank between two voltage pulse generations. The capacitor bank provides all the pulse energy and its

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14. ABSTRACT
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15. SUBJECT TERMS

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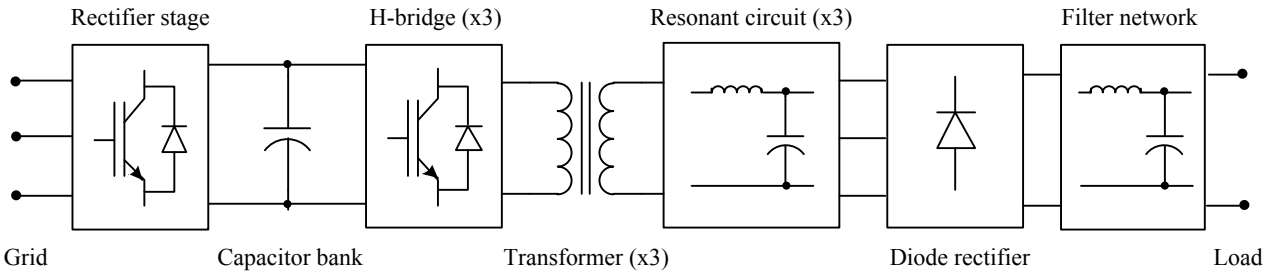

Figure 1. Generalised block diagram of the pulsed power SRPL resonant converter modulators.

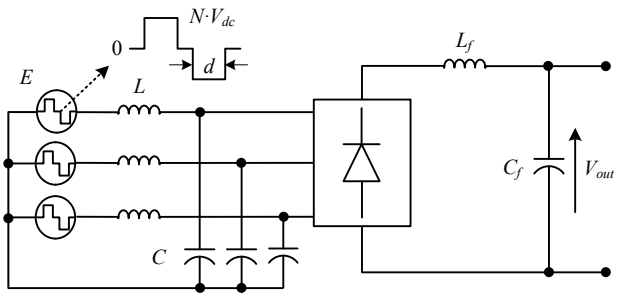

Figure 2. Simplified equivalent circuit of the three-phase fully resonant variant.

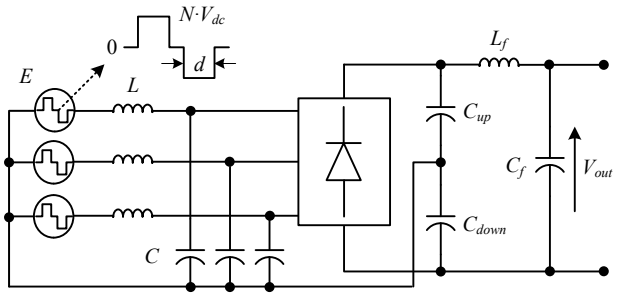

Figure 3. Simplified equivalent circuit of the Y-point connected part resonant variant.

voltage level drops considerably to avoid low frequency disturbances on the grid (i.e. due to nature of transient load demands). Three single phase H-bridge inverters are employed to produce three 20kHz square wave voltages with 120° relative phase shift. Three single phase high frequency transformers are utilized to boost the voltage to the level that is required by the load. A SRPL tank approach is selected to further amplify the voltage and to achieve low losses of semiconductor devices through soft-switching. A high voltage three-phase diode bridge rectifier and filter network are used to attain a low ripple output.

As the input rectifying stage is modulated to charge the DC-link capacitor bank only when the output voltage pulse is null, it can be excluded from the scope of design and operation analysis. Fig. 2 and Fig. 3 present the simplified equivalent circuits of the two converter variants, where N is the transformer turns ratio (secondary turns over primary turns); V_{dc} is the DC-link capacitor voltage; E is the H-bridge output voltage referred to the transformer secondary winding (with duty cycle of d and amplitude of NV_{dc}); L and C represent the inductance and capacitance of the resonant circuit; An LC filter (L_f and C_f) is employed to attain a low ripple output V_{out}.

The main difference between the two variants is the operating condition of the resonant circuit: for the part resonant variant, the neutral point formed by the three transformers is connected with the center point of an output split DC capacitance (C_{up} and C_{down}), and thereby the converter is operated in the resonant mode for less than 40% of the cycle [8]; for the fully resonant variant, the frequency of the square wave voltages is reasonably close to the tank resonant frequency, and thus the converter is operated in the fully resonant mode. The detailed operation analysis and optimization algorithms of the two converter variants can be found in [3, 4, 8].

In this work, the two converter variants are designed and optimized to produce a set of 9MW, 120kV, 1ms, 1% ripple voltage pulses, when supplied by a 2.4kV DC-link capacitor. A 15% droop level is considered for the capacitor voltage, the value which is chosen as a compromise between the converter volume and VA rating. Table 1 and Table 2 summarize the parameters of

Table 1. Parameters of the fully resonant variant.

Symbol	Description	Value
C_{dc}	DC-link capacitor	11.3mF
N	Transformer turns ratio	9.3
L	Resonant inductance	2.1mH
C	Resonant capacitance	25nF
L_f	Filter inductance	7.2mH
C_f	Filter capacitance	2.8nF
Q	Tank quality factor	3
f	Nominal switching frequency	20kHz

Table 2. Parameters of the part resonant variant.

Symbol	Description	Value
C_{dc}	DC-link capacitor	11.3mF
N	Transformer turns ratio	15
L	Resonant inductance	3.2mH
C	Resonant capacitance	11.4nF
L_f	Filter inductance	3.38mH
C_f	Filter capacitance	1.32nF
C_{up}/C_{down}	Split DC capacitance	30nF(x2)
f	Nominal switching frequency	20kHz

the two converter variants.

III. MODELING

Compared to conventional converters, the modeling process of the pulsed power resonant converters is much different. Due to the resonant stage introduced, there are high frequency state variables (e.g. resonant inductor currents) existing in the converter circuit. Traditional approaches, such as the state space averaging and the averaged switch modeling, are of less effect.

For the fully resonant variant, the DQ modeling has been demonstrated in [9] as an effective modeling approach. Following a similar procedure and taking the transformer turns ratio into account, the DQ model for the fully resonant variant can be obtained. Fig. 4 shows the output comparison of the converter model and the developed DQ model. Simulations have been undertaken in an open loop case with a fixed DC-link voltage (i.e. the influence of the DC-link voltage droop is neglected). The good match in the dynamic responses of the two models confirms the accuracy of the DQ modeling.

Due to the connection between the transformer neutral (i.e. the Y-point) and the center point of the output split DC capacitance, the part resonant variant is only operated at the resonant mode for a specific period of each cycle, which makes the converter modeling very difficult. Based on the converter step response, a second order transfer function is considered to approximately represent the converter. Fig. 5 shows the output comparison of the converter model and the second order transfer function model. As it can be seen, the proposed transfer function represents the part resonant variant functionally though a slight mismatch in the dynamics can be observed.

It is necessary to appreciate that the proposed models for the two converter variants should be carefully used when designing the converter control. This is because, during the pulse generation, the three H-bridge inverters are required to be operated with varying frequency and phase shift, in order to compensate the effect of the significant DC-link voltage droop. This important feature brings a continuously changing dynamics and voltage transfer ratio (i.e. ratio of the output voltage to the DC-link voltage). Although the range of the operating frequency is relatively small (i.e. a few kilohertz), the differences in the dynamics and voltage transfer ratio can introduce model uncertainties, which will downgrade the closed-loop control performance to some extent. In order to obtain good control performance both in transient and steady state conditions, the novel PI + RC strategy is proposed and discussed in Section IV.

IV. PULSE VOLTAGE CONTROL

Considering the stringent pulse quality requirements, the following conditions are imposed to the output voltage control of the two converters: firstly, the pulse rise time should be less than 100μs to ensure high conversion efficiency; secondly, the pulse overshoot should be less than 3%; thirdly, the pulse amplitude should be kept flat despite the DC-link voltage is drooping significantly.

The use of traditional controllers, such as PI or PID, on their own is not sufficient to achieve a successful implementation, due to model uncertainties, but also to the high control bandwidth required. The multi-variable state feedback controller proposed in [9] can regulate the pulse amplitude effectively, but the rise time was longer than expected, affected mainly by the influence of the varying frequency operation on the full state observer. In this work, the PI + RC control strategy is considered for the two converter variants.

In the past two decades, RC has been widely used for feedback control systems that are subject to periodic inputs. Based on the internal model principle (IMP) [10], it uses the error signal of previous cycle to improve the performance of current cycle. Theoretically, with a suitable designed RC, the output of a stable feedback system can track the periodic inputs (reference or/and disturbance) with zero steady state error, even in the presence of model uncertainties [11].

Fig. 6 presents the proposed PI + RC voltage control strategy. For the two converter variants, the PI controller needs to be designed first to ensure the system is sufficiently closed-loop stable. Since any overshoot at the pulse beginning is undesirable, a large damping ratio (i.e. 0.9) is considered to give a close-to-critical damping.

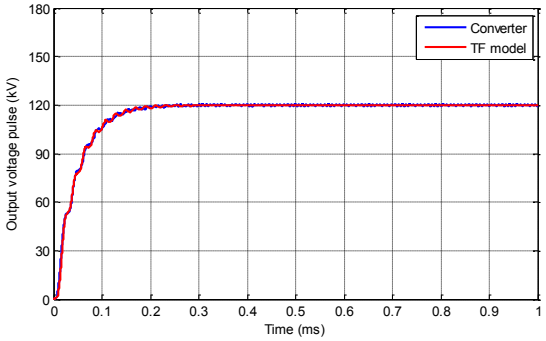

Figure 4. Fully resonant variant: output comparison of the converter and TF model with fixed DC-link.

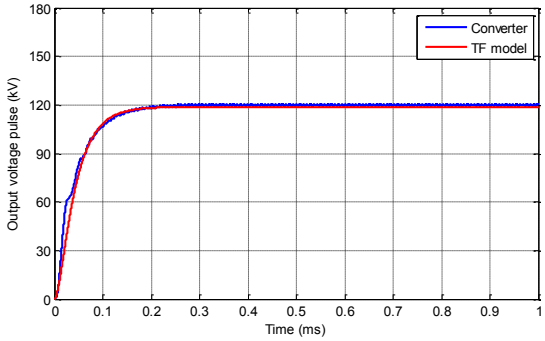

Figure 5. Part resonant variant: output comparison of the converter and TF model with fixed DC-link.

With only the PI controller, the large droop of the DC-link voltage can be compensated, so that the pulse amplitude can be kept flat. However, due to the large damping ratio, the pulse rise time will exceed the specification requirements.

The aim of RC is to reduce the pulse rise time cycle by cycle, eventually towards the converter physical limitation, while the overshoot remains small. As illustrated in Fig. 7, the difference between the ideal pulse and the output pulse regulated by the PI controller can be treated as the periodic error. Based on the IMP, zero tracking error can be achieved in steady state if the periodic error signal is included inside the stable closed-loop system [12].

The RC design demands careful considerations and needs to be tailed for this specific application. K_{RC} is the repetitive learning gain. Either too small or too large value of it can cause slow convergence or reduced robustness. z^{-M} is the delay line, where M is the ratio between the pulse period T_p and the sampling time T_s. The robustness filter $Q(z)$ is chosen to be a close-to-unity constant (e.g. 0.9), in order to modify the internal model and thus increase the system stability margin. A time advance unit is selected as the stability filter $G_f(z)$ to ensure the overall system is stable after the introduction of RC. Table 3 and Table 4 summarize the control parameters of the two converter variants.

V. MODULATION

It has been demonstrated that employing frequency or phase shift modulation alone is not possible to maintain the soft-switching of the IGBTs throughout the pulse generation [2, 3]. Due to the high power rating of the voltage pulses, devices hard-switching leads to a steep increment on the switching losses and thus sacrifices the system efficiency largely. In order to overcome that, the combined frequency and phase shift modulation approach is selected to modulate the two converters.

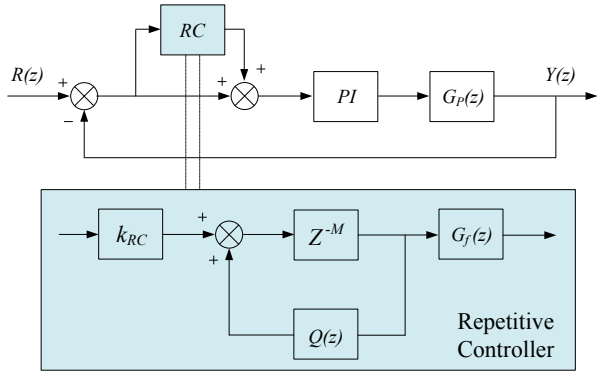

Figure 6. Proposed PI + RC voltage control strategy.

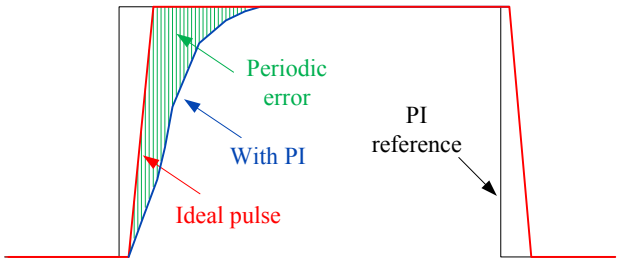

Figure 7. Periodic error signal seen by RC.

For the fully resonant variant, the fundamental component of the square wave voltages is considered to drive the input of the resonant circuit (i.e. fundamental mode approximation), since the selective resonant circuit (i.e. Q=3) is employed and the converter is switched around the resonant frequency f_r. Based on that, the relationship between the phase shift φ of the two halves of H-bridge (i.e. $\varphi=\pi-d$) and the switching frequency for a zero current switching can be derived as in Eq. (1).

$$\varphi=2atan\left(Q\frac{f_s^3}{f_r^3}+\frac{f_s}{Qf_r}-Q\frac{f_s}{f_r}\right) \quad (1)$$

The analysis of the Y-point connected part resonant variant under the combined frequency and phase shift modulation has been presented in [8]. For the zero current switching, the relationship between the phase shift and the switching frequency can be expressed as in Eq. (2).

$$f_s=\frac{\frac{\varphi NV_{dc}}{\pi}-NV_{dc}+\frac{V_{out}}{2}}{\left[NV_{dc}\left(2-\pi\right)+\frac{V_{out}}{2}\left(2+\pi\right)\right]\sqrt{LC}} \quad (2)$$

With the instantaneous DC-link voltage V_{dc} returned by the measurement and the generated feedback control signal V_C, the phase shift and the corresponding switching frequency for the three H-bridge inverters can be determined. Under this modulation scheme, the influence of the DC-link voltage droop can be compensated, while the soft-switching of the IGBTs can be always achieved. Fig. 8 shows a generalized modulation block diagram for the two converters.

Table 3. Control parameters of the fully resonant variant.

Symbol	Description	Value
f_s	Sampling frequency	40kHz
K_P	PI parameter K_P	0.018
K_I	PI parameter K_I	0.007
K_{RC}	RC learning gain	0.5
M	Delay line	40
$G_f(z)$	Stability filter	z^2

Table 4. Control parameters of the part resonant variant.

Symbol	Description	Value
f_s	Sampling frequency	40kHz
K_P	PI parameter K_P	0.015
K_I	PI parameter K_I	0.006
K_{RC}	RC learning gain	0.35
M	Delay line	40
$G_f(z)$	Stability filter	z^1

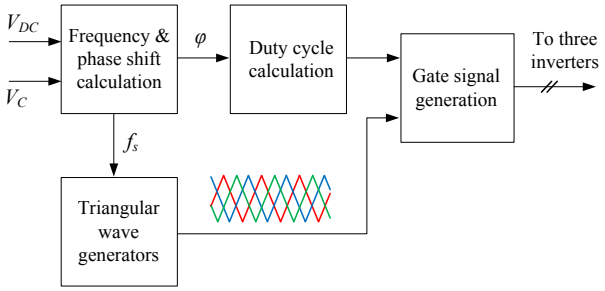

Figure 8. Generalized modulation block diagram.

VI. SIMULATION RESULTS

For purpose of verification, the two converter variants have been tested by using the PLECS platform. Fig. 9 to Fig. 12 show the DC-link voltages and output voltage pulses of the two variants, respectively in the first repetition, where only the PI controller is active. For both cases, the pulse amplitude is maintained flat, whilst the DC-link voltage drops constantly. The droop level is about 15%, the value of which confirms the converter design. Due to the large damping ratio of the PI controller, the pulse rise time is much longer than required, which implies the necessity of RC.

RC takes action from the generation of the second pulse. Fig. 13 and Fig. 14 shows the output voltage pulses of the two converter variants in the twentieth repetition, where the RCs have reached the steady state. Clearly, the rise time for the both cases is improved significantly by means of the RC, while the overshoot remains negligible. The rise time for the fully resonant variant is about 72µs, and is even shorter, 43µs, for the part resonant variant.

Fig. 15 and Fig. 16 show the switching waveforms of Phase A of the two variants. The plotting window is chosen around the center of the twentieth pulse. It can be seen that, the three H-bridge inverters have been always switched at the zero-crossing of the current (ZCS). In practical applications, a snubber capacitor can be used to slow down the rate of voltage rise and achieve an operating condition close to zero-voltage switching-off (ZVS) [5]. As a result, the soft-switching can be achieved in all IGBTs throughout the pulse duration.

VII. CONCLUSION

The two classical pulsed power SRPL resonant converters have been designed and optimized for RF applications. The novel PI + RC closed-loop control strategy has been employed for voltage pulse regulation, resulting in a fast rise time, reduced overshoot and constant amplitude. The combined frequency and phase shift modulation has been used to ensure the soft-switching of the IGBTs throughout the pulse generation. The simulation results confirm the converter design, modeling method, control strategy and modulation approach of the two converter variants.

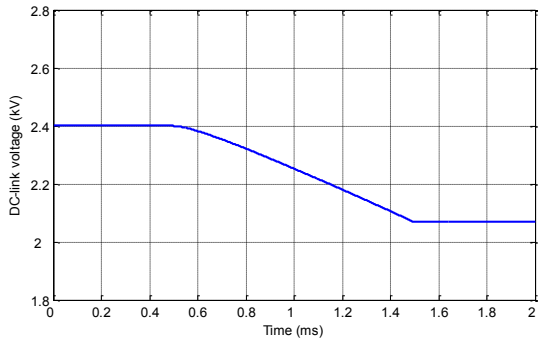

Figure 9. DC-link voltage of the fully resonant variant.

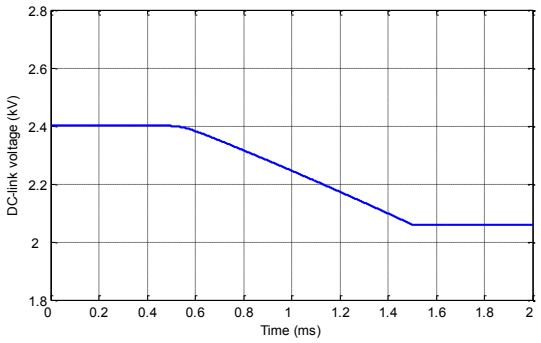

Figure 10. DC-link voltage of the part resonant variant.

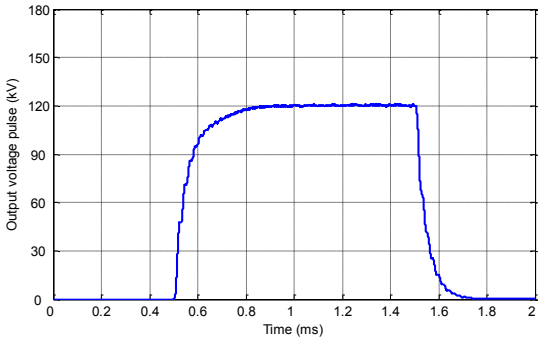

Figure 11. Fully resonant variant: 1st voltage pulse with PI control only.

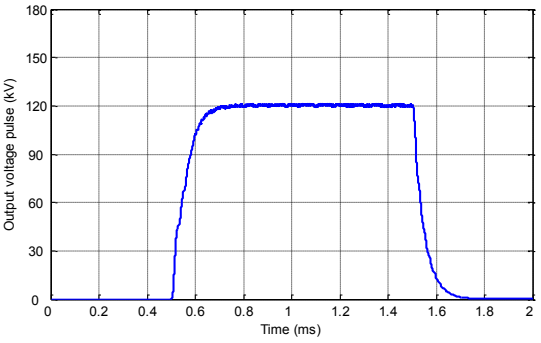

Figure 12. Part resonant variant: 1st voltage pulse with PI control only.

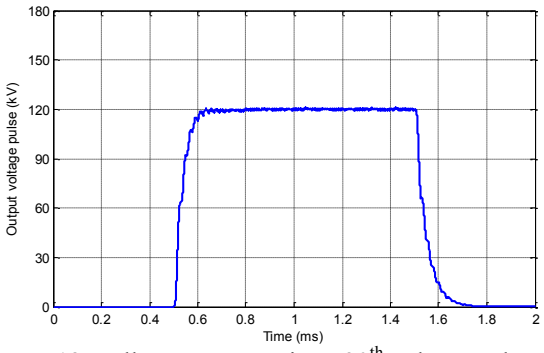

Figure 13. Fully resonant variant: 20th voltage pulse with PI + RC control.

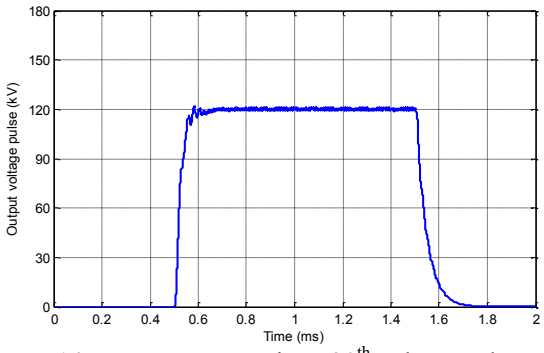

Figure 14. Part resonant variant: 20th voltage pulse with PI + RC control.

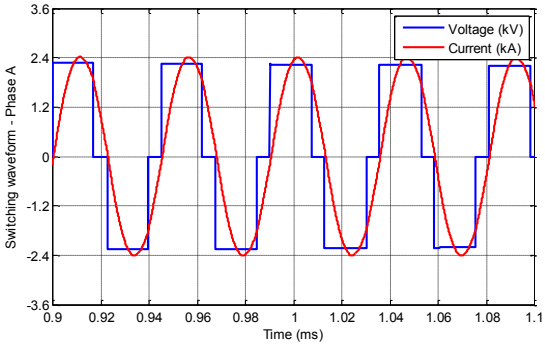

Figure 15. Fully resonant variant: switching waveform of Phase A at the 20th voltage pulse.

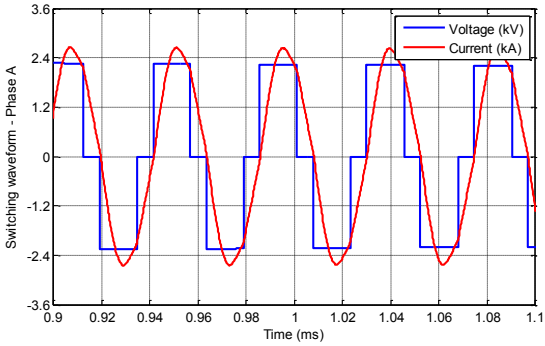

Figure 16. Part resonant variant: switching waveform of Phase A at the 20th voltage pulse.

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